CLAIMS

1. (Currently amended) A memory system, comprising:

a first buffer chip directly mounted on a motherboard;

at least one first memory ~~device~~ chip coupled to the first buffer and directly mounted ~~to~~ on the motherboard; and

a plurality of signal traces routed on the motherboard to the first buffer and the at least one first memory chip ~~device~~;

where the system eliminates signal reflection caused by signal trace discontinuities between the first buffer and the at least one first memory device by directly mounting the first buffer and the at least one first memory device on the motherboard without an intervening socket.

2. (Currently amended) The memory system of claim 1 where the first buffer chip is a command and address buffer capable of driving the at least one first memory ~~device~~ chip with address and command signals.

3. (Original) The memory system of claim 2 where the command and address buffer receives a command and address signal through a first command and address signal trace routed on the motherboard.

4. (Currently amended) The memory system of claim 3

where the at least one first memory ~~device~~ chip receives the command and address signals outputted from the command and address buffer through a second command and address signal trace routed on the motherboard; and

where the first command and address signal trace is arranged substantially ~~perpendicularly with~~ perpendicular to the second command and address signal trace.

5. (Currently amended) The memory system of claim 1 where the at least one first memory ~~device~~ chip is one of a DRAM and SDRAM.

6. (Currently amended) The memory system of claim 1 where the at least one first memory ~~device~~ chip receives a data signal and a clock signal through corresponding data and clock signal traces routed on the motherboard.

7-14. (Canceled)

15. (Currently amended) A memory system, comprising:

at least one memory rank mounted directly on a motherboard; and

a plurality of signal traces routed on the motherboard to the at least one memory rank;

where the system eliminates signal reflection caused by signal trace discontinuities between the at least one memory rank and the plurality of signal traces by directly mounting the at least one memory rank on the motherboard.

16. (Original) The memory system of claim 15 where the at least one memory rank comprises:

at least one first memory device; and

a first buffer capable of driving address and command signals to the at least one first memory device through corresponding signal traces routed on the motherboard.

17. (Currently amended) The memory system of claim 16 where the ~~at least one~~ first buffer receives a command and address signal through a first command and address signal trace routed on the motherboard.

18. (Currently amended) The memory system of claim 17

where the at least one first memory device receives the command and address signal outputted from the ~~at least one~~ first buffer through a second command and address signal trace routed on the motherboard; and

where the first command and address signal trace is arranged substantially ~~perpendicularly with~~ perpendicular to the second command and address signal trace.

19. (Original) The memory system of claim 17 where the at least one first memory device receives a data signal and a clock signal through corresponding data and clock signal traces routed on the motherboard.

20. (Original) The memory system of claim 17 where the at least one first memory device is one of a DRAM and SDRAM.

21-38. (Canceled)

39. (Currently amended) A memory system, comprising:

a memory controller mounted directly on a motherboard and generating a plurality of command and address signals;

a first buffer mounted directly on the motherboard and receiving the command and address signals;

at least one first memory device coupled to the first buffer and mounted directly ~~to~~ on the motherboard; and

a plurality of signal traces routed on the motherboard to the first buffer and the at least one first memory device;

where the system eliminates signal reflection caused by signal trace discontinuities between the memory controller, the first buffer, the at least on first memory, and the plurality of signal traces by directly mounting the memory controller, the first buffer, the at least on first memory, and the plurality of signal traces on the motherboard.

40-42. (Canceled)